WHAT IS CLAIMED IS:

1. A method of manufacturing a semiconductor integrated circuit device including a plurality of word lines formed over a semiconductor substrate, a plurality of bit lines disposed so as to be transverse to said plurality of word lines, and memory cells each disposed at one of intersections between said plurality of word lines and said plurality of bit lines, each of said memory cells including a memory cell selection transistor having a gate electrode formed by a part of one of said word lines and an information storage capacitor having a principal part disposed over one of said bit lines, a first semiconductor region of said memory cell selection transistor being electrically connected to said information storing capacitor, and a second semiconductor region of said memory cell selection transistor being electrically connected to one of said bit lines, the method comprising the steps of:

(a) covering upper and side surfaces of each of said plurality of word lines with first insulating films;

(b) forming a second insulating film on said semiconductor substrate to cover therewith said first insulating films, said second insulating film being made of a material larger in etching rate than a material of said first insulating films;

(c) forming a first mask film on said second insulating film, said first mask film being made of a material smaller in etching rate than the material of said second insulating film, and thereafter forming openings in first contact hole forming regions of said first mask film;

(d) forming first contact holes by using said first mask film as an etching mask so as to expose said first semiconductor regions of said memory cell selection transistors, said first contact holes being defined by said first insulating films in self-alignment;

(e) forming said bit lines by forming a first conductor film on the resulting

semiconductor substrate after forming said first contact holes and then patterning said first conductor film;

(f) covering upper and side surfaces of said bit lines with third insulating films, said third insulating films being made of a material substantially equal in permittivity to the material of said first insulating films, said third insulating films being formed so as to be thicker than said first insulating films;

(g) covering said third insulating films with a fourth insulating film, said fourth insulating film being made of a material larger in etching rate than the material of said first insulating films;

(h) forming a second mask film on the upper surface of said fourth insulating film, said second mask film being made of a material smaller in etching rate than the material of said fourth insulating film, and thereafter forming openings in second contact hole forming regions of said second mask film;

(i) after said step of forming openings in said second mask film, forming a side wall mask film made of a material smaller in etching rate than the material of said fourth insulating film, then etching back the side wall mask film, thereby forming side wall films including portions of said side wall mask films on side surfaces defining openings of said second mask film;

(j) forming second contact holes so as to expose the second semiconductor regions of said memory cell selection transistors by conducting etching processing using said second mask film and side wall films as an etching mask, wherein said etching processing is conducted as a series of etching steps including (1) conducting anisotropic etching processing with non-selectivity for a material of the first insulating film to form an upper part of holes of said second contact holes up to such a depth as not to reach said second insulating film, and (2) conducting etching processing with selectivity for the first insulating film to form a

lower part of the second contact holes extending from said upper part of holes and reaching said second semiconductor regions through said second insulating film with said first insulating films being retained as a self-alignment etching mask, thereby forming said second contact holes by using said first insulating films; and

(k) forming a part of a first electrode of said information storing capacitor by forming a second conductor film on the resulting semiconductor substrate after forming said second contact holes and then patterning said second conductor film.

2. A method according to claim 1, further comprising:

(l) after covering upper and side surfaces of said bit lines with said third insulating films, forming a fifth insulating film serving as an etching stopper on said second insulating film to cover therewith said third insulating films; and

(m) forming said fourth insulating film on said fifth insulating film serving as the etching stopper,

wherein when forming said second contact holes so as to expose the second semiconductor regions of said memory cell selection transistors by conducting etching processing using said second mask film and said side wall films as an etching mask, the depth of said upper part of holes of said second contact holes formed by said anisotropic etching processing corresponds to such a position that said fifth insulating film serving as the etching stopper has been etched lastly.

3. A method according to claim 2, wherein said first insulating films and said third insulating films are made of silicon nitride.

4. A method of manufacturing a semiconductor device, comprising the steps of:

forming first conductors over a main surface of a semiconductor substrate with a first insulating film interposed therebetween;

forming semiconductor regions in said main surface of the semiconductor substrate on both sides of said first conductors;

covering upper and side surfaces of said first conductors with second insulating films, thereby providing a resulting substrate;

forming a third insulating film of larger etching rate than that of said second insulating film on the resulting substrate;

forming first contact holes by etching through said third insulating film for first ones of said semiconductor regions;

forming second conductors extending to contact with said first ones of said semiconductor regions through said first contact holes and extending on said third insulating film in a direction transverse to said first conductors;

covering upper and side surfaces of said second conductors with fourth insulating films of smaller permittivity than that of said second insulating film;

forming a sixth insulating film on said third insulating film and on said fourth insulating film, of same permittivity as that of said second insulating film:

forming a fifth insulating film on said sixth insulating film;

forming a patterned mask film on said fifth insulating film, said patterned mask film having side walls defining openings substantially aligned with second ones of said semiconductor regions;

forming a side wall film on each of said side walls of said patterned mask film to narrow said openings in said patterned mask film; and

forming second contact holes, by etching through said fifth insulating film, said sixth insulating film and said third insulating film for second ones of said semiconductor regions, using said patterned mask with said side wall films.

5. A method according to claim 4, wherein said fourth insulating films are of silicon oxide and said sixth insulating film is of silicon nitride.

6. A method according to claim 4, further comprising the steps of:

forming conductive films on said second ones of said semiconductor regions and on inner walls of said second contact holes; and

forming capacitors over said second ones of said semiconductor regions, with said conductive films used as electrodes of said capacitors.

7. A method of manufacturing a semiconductor device, comprising the steps of:

forming first conductors over a main surface of a semiconductor substrate with a first insulating film interposed therebetween;

forming semiconductor regions in said main surface of the semiconductor substrate on both sides of said first conductors;

covering upper and side surfaces of said first conductors with second insulating films, thereby forming a resulting substrate;

forming a third insulating film of larger etching rate than that of said second insulating film on the resulting substrate;

forming first contact holes by etching through said third insulating film for first ones of said semiconductor regions;

forming second conductors extending to contact with said first ones of semiconductor regions through said first contact holes and extending on said third insulating film in a direction transverse to said first conductors;

covering upper and side surfaces of said second conductors with fourth insulating films of same permittivity as that of said second insulating films but of a

larger thickness than that of said second insulating film;

forming a fifth insulating film on said third insulating film and on said fourth insulating films;

forming a patterned mask film on said fifth insulating film, said patterned mask film having side walls defining openings substantially aligned with second ones of said semiconductor regions;

forming a side wall film on each of said side walls of said patterned mask film to narrow said openings in said patterned mask film; and

forming second contact holes, by etching through said fifth insulating film and said third insulating film, for second ones of said semiconductor regions, using said patterned mask with said side wall films as a mask.

8. A method according to claim 7, further comprising the steps of:

forming conductive films on said second ones of said semiconductor regions and on inner walls of said second contact holes; and

forming capacitors over said second ones of said semiconductor regions, with said conductive films used as electrodes of said capacitors.